Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A manufacturing method for a semiconductor device comprising:

semi-full dicing a semiconductor wafer so as to leave a dicing residual portion with a predetermined thickness between devices on the semiconductor wafer;

providing a protective layer having a chemical etching resistant property on an element formation face of the semiconductor wafer, wherein the protective layer is bonded to the semiconductor wafer using a bonding agent having a chemical etching resistant property and a protective layer holding means is placed on a peripheral portion of the protective layer so as to surround the entire circumference of the semiconductor wafer; and

chemically etching the semiconductor wafer having the protective layer provided on the element formation face from the rear face side so as to polish the rear face of the semiconductor wafer, to remove the dicing residual portion to divide the semiconductor wafer into individual semiconductor chips, and to remove damaged areas in a cut face of the semiconductor wafer resulting from the semi-full dicing process,

wherein the protective layer holding means has draining means for draining etchant remaining inside the protective layer holding means during the chemical etching and the draining means is formed as grooves in the protective layer holding means which extend in a radial manner.

Claim 2 (Previously Presented): The manufacturing method for a semiconductor device as defined in claim 1, further comprising:

prior to the semi-full dicing, carrying out an electrical test on the semiconductor wafer by means of probing.

Claim 3 (Previously Presented): The manufacturing method for a semiconductor device as defined in claim 1, further comprising:

removing the protective layer from the semiconductor chips after the chemical etching.

Claim 4 (Previously Presented): The manufacturing method for a semiconductor device as defined in claim 1, wherein in the semi-full dicing, the semiconductor wafer is subjected to semi-full dicing from the element formation face so as to leave a dicing residual portion with a predetermined thickness on the rear face side of the semiconductor wafer.

Claim 5 (Canceled)

Claim 6 (Withdrawn): The manufacturing method for a semiconductor device as defined in claim 1, wherein in the semi-full dicing ~~step~~, the semiconductor wafer is subjected to semi-full dicing from the rear face so as to leave a dicing residual portion with a predetermined thickness on the element formation face side of the semiconductor wafer.

Claims 7 and 8 (Canceled).

Claim 9 (Previously Presented): The manufacturing method for a semiconductor device as defined in claim 1, wherein the protective layer is a film.

Claim 10 (Previously Presented): The manufacturing method for a semiconductor device as defined in claim 1, wherein the protective layer is a chemical

etching resistant film of an ultraviolet separation type, which has a reduction in adhesive strength upon irradiation with ultraviolet rays.

Claim 11 (Previously Presented): The manufacturing method for a semiconductor device as defined in claim 1, wherein the protective layer is a chemical etching resistant film of a thermal type, which has a reduction in adhesive strength upon application of heat.

Claim 12 (Original): The manufacturing method for a semiconductor device as defined in claim 1, wherein the protective layer is a chemical etching resistant film of a sticking type, which has an adhesive strength that allows the individually divided semiconductor chips to be separated from the protective layer one by one.

Claim 13 (Currently Amended): The manufacturing method for a semiconductor device as defined in claim 1, wherein the protective layer holding means holds ~~further comprising holding~~ the protective layer with a uniform tension during the chemical etching.

Claim 14 (Canceled).

Claim 15 (Currently Amended) The manufacturing method for a semiconductor device as defined in claim 1 ~~13~~, wherein ~~the~~ uniform tension is maintained on the ~~said~~ protective layer by the ~~a~~ protective layer holding means and wherein the protective layer holding means is placed on the same surface of the ~~said~~ protective layer as the semiconductor wafer.

Claim 16 (Currently Amended) The manufacturing method for a semiconductor device as defined in claim 1, wherein the ~~further comprising placing a~~ protective layer holding means has ~~having~~ a chemical etching resistant property ~~on a~~

~~peripheral portion of the protective layer so as to surround the entire circumference of the semiconductor wafer.~~

Claim 17 (Currently Amended): The manufacturing method for a semiconductor device as defined in claim 1 ~~16~~, wherein the protective layer holding means has a ring shape with a flat bonding face for bonding with the protective layer.

Claim 18-42(Canceled).

Claim 43 (Previously Presented): A method for manufacturing a semiconductor device comprising:

dicing a semiconductor wafer so as to leave a residual portion with a predetermined thickness between devices on the semiconductor wafer;

providing a protective layer having a chemical etching resistant property on an element formation face of the semiconductor wafer, wherein the protective layer is bonded to the semiconductor wafer using a bonding agent having a chemical etching resistant property and wherein a protective layer holder with radially-extending grooves formed therein is attached to a peripheral portion of the protective layer;

chemically etching with etchant the semiconductor wafer having the protective layer provided on the element formation face from the rear face side so as to polish the rear face of the semiconductor wafer, to remove the residual portion to divide the semiconductor wafer into individual semiconductor chips, and to remove damaged areas on portions of the semiconductor wafer exposed by the dicing; and

draining residual etchant from the protective layer holder via the radially-extending grooves formed therein.

Claim 44 (Previously Presented): The method as defined in claim 43, further comprising;

electrically testing the semiconductor wafer prior to dicing.

Claim 45 (Previously Presented): The method as defined in claim 43, further comprising:

removing the protective layer from the semiconductor chips after the chemical etching.

Claim 46 (Previously Presented): The method as defined in claim 45, wherein the protective layer is removed using ultraviolet irradiation.

Claim 47 (Previously Presented): The method as defined in claim 45, wherein the protective layer is removed using heat.

Claim 48 (Previously Presented): The method as defined in claim 43, wherein the dicing of the semiconductor wafer is from the element formation face so as to leave the residual portion with a predetermined thickness on the rear face side of the semiconductor wafer.

Claim 49 (Previously Presented): The method as defined in claim 43, wherein the protective layer is a chemical etching resistant film of a thermal type, which has a reduction in adhesive strength upon application of heat.